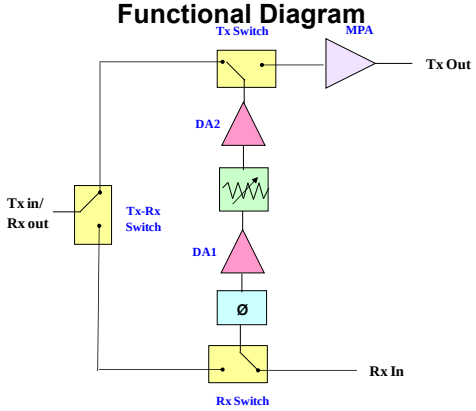
8.7 – 10.5 GHz GaAs MMIC Core Chip

Features

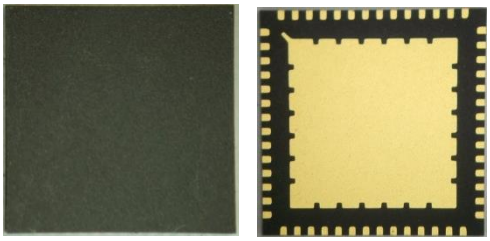
- **Frequency Range: 8.7GHz – 10.5GHz**
- **Tx Small Signal Gain: 25dB**
- **Rx Small Signal Gain: 2.5dB**
- **Tx Output P_{1dB} : 21dBm**
- **Tx Output P_{sat} : 22dBm**
- **Phase Shifter Range : 6 Bit, 5.625˚ step**
- **Attenuator Range : 6 Bit, 0.5dB step**
- **0.5 µm InGaAs pHEMT Technology**
- **Open Cavity QFN Package**
- **Package dimension: 8mmx8mmx0.8mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **VSAT**



Description

The ASL6001OP is a multi-functional Transmit / Receive 3 port core chip. It is designed for applications operating within the 8.7 GHz to 10.5 GHz range. This core chip consists of integrated transmit/receive switches, 6-bit phase shifter, 6-bit attenuator, gain blocks and medium power amplifier. The digital control logic allows fast phase shift and attenuation changes. This device is well suited for phased array radar applications.

The package used is a SMD open cavity QFN Package with base metal made up of copper composite.

Absolute Maximum Ratings[1]:

Parameter	Absolute Maximum	Units
Supply Voltage (DA1VD, DA2VD, VDMPA)	6	V
Control Logic Supply & Gate Supply for DA1 and DA2 (-5V / -5VOPT1 / -5VOPT2)	-6 to -4	V
Gate Voltage of MPA (VGMPA)	-0.6 to -2.5	V
Control Logic Supply (5V / 5VOPT1 / 5VOPT2)	0 to 5.5	V
RF input at Tx_{in} Port	17 @ 85 °C	dBm
RF input at Rx_{in} Port	17 @ 85 °C	dBm
Supply current in Tx Mode	380	mA
Supply current in Rx Mode	150	mA
Operating temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C

1. Operation beyond these limits may cause permanent damage to the component

Test fixture data[2]:

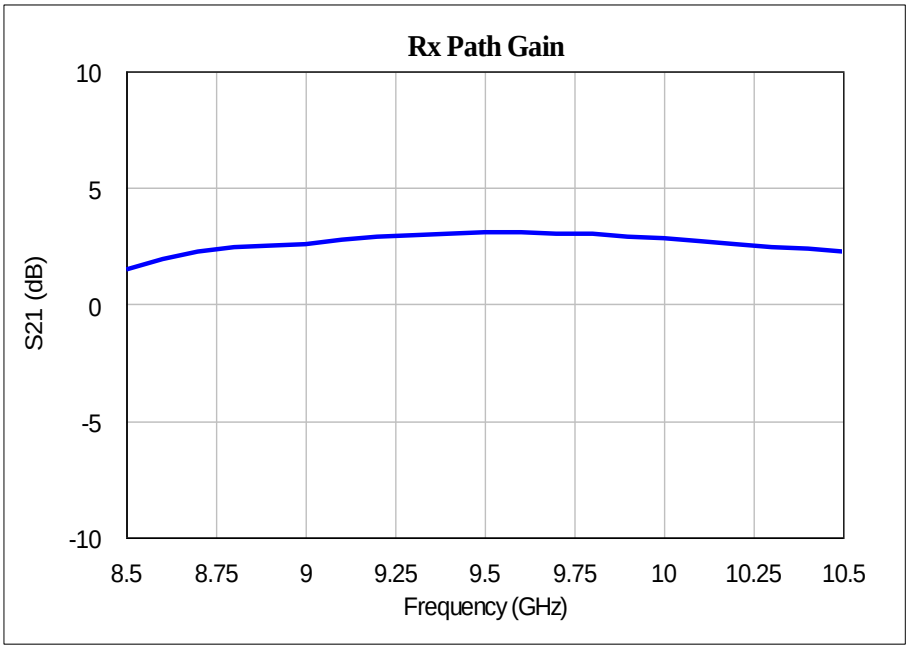
VDDA1 = VDDA2 = VDMPA = 5V; VGMPA=-0.9V ; T_A = 25 °C

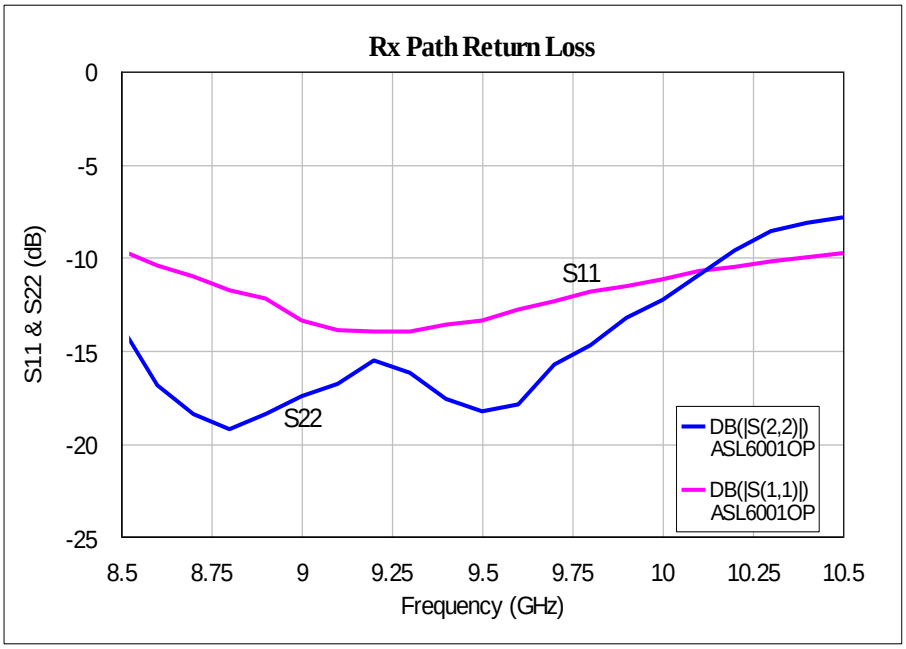
Parameter	Min	Typ	Max	Units
Frequency Range	8.7		10.5	GHz
Receive Mode Small Signal Gain	1.5	2.5		dB
Transmit Mode Small Signal Gain	23	25		dB
Transmit Mode Large Signal Gain (@ Pin = 0dBm)	20.5	22		dB
Input / Output Return Losses	8	10		dB
Receive Mode Output Power for 1dB Compression Point		12		dBm
Receive Mode Output Third Order Intercept Point		22		dBm
Receive Mode Noise Figure		15		dB
Transmit Mode Output Power for 1dB Compression Point	19.5	21		dBm
Transmit Mode Output Saturated Power	20.5	22		dBm
Phase Shifter Range (6 Bit, 64 states, 5.625° step)		0 – 355		deg
RMS Phase Error - Calibrated		3.5@9-10GHz		deg
RMS Phase Error - UnCalibrated		3.9@9-10GHz		deg
Attenuation Range (6 Bit, 64 states, 0.5dB step)		0 – 31.5		dB
RMS Attenuation Error - Calibrated		0.55@9-10GHz		dB
RMS Attenuation Error - UnCalibrated		0.8@9-10GHz		
Tx/Rx Switch Isolation		< -57		dB
Tx/Rx Switch Switching Time		< 50		ηSec
Supply Voltages		5, -5, -0.9		V
Average Current (10%Duty@TxMode & 90%Duty@RxMode)	Tx Path	~ 110		mA
	Rx Path	~ 80		
Supply Current (CW Mode)	Tx Path	~ 300		mA
	Rx Path	~ 88		
TTL Control Voltage (OFF / ON)		0 / 3.3	0 / 5.5	V
Chip Size		5.3 x 5.3		mm

2. Electrical specifications are measured in a test fixture

Test fixture data in Rx mode (Tx/Rx Control = 0V); Duty cycle = 90%:

VDDA1 = VDDA2 = 5V ; Total Current ($I_{DDA1Avg}$ + $I_{DDA2Avg}$) = 80mA, T_A = 25 °C





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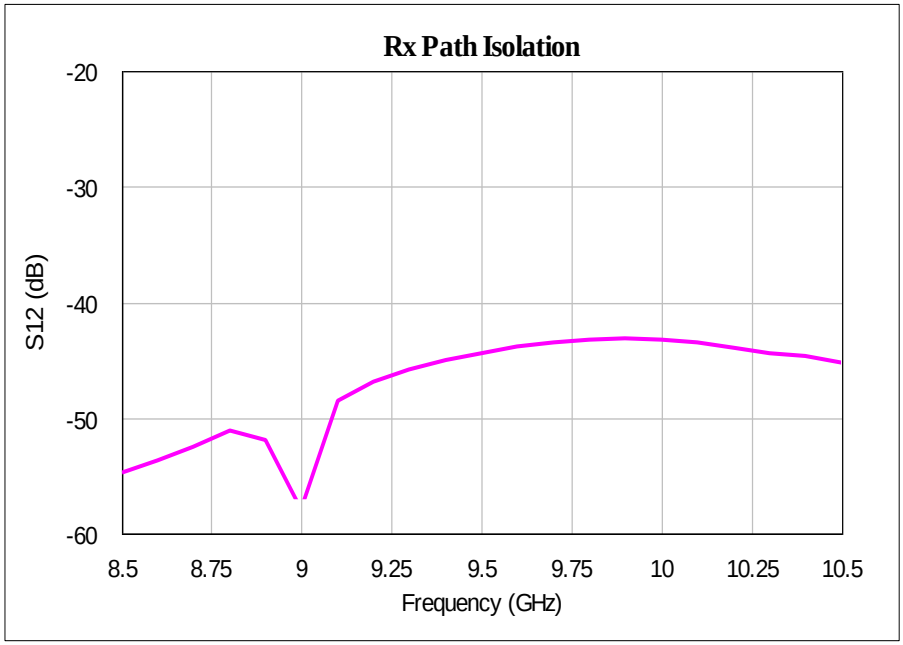

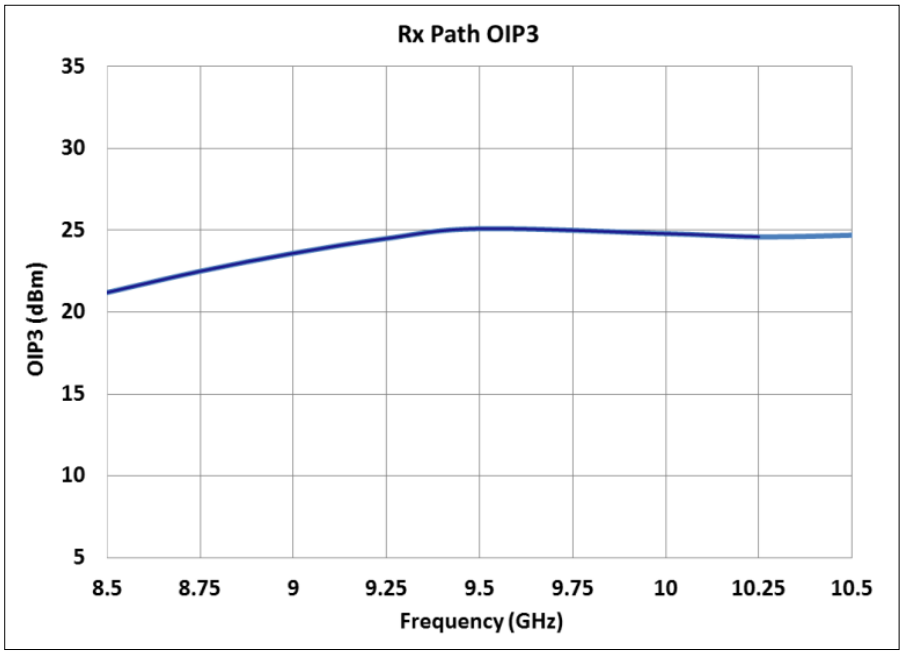

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VDDA1 = VDDA2 = 5V ; Total Current ($I_{DDA1Avg}$ + $I_{DDA2Avg}$) = 80mA, T_A = 25 °C

6 Bit Digital Phase Shifter Performance (only prime states):

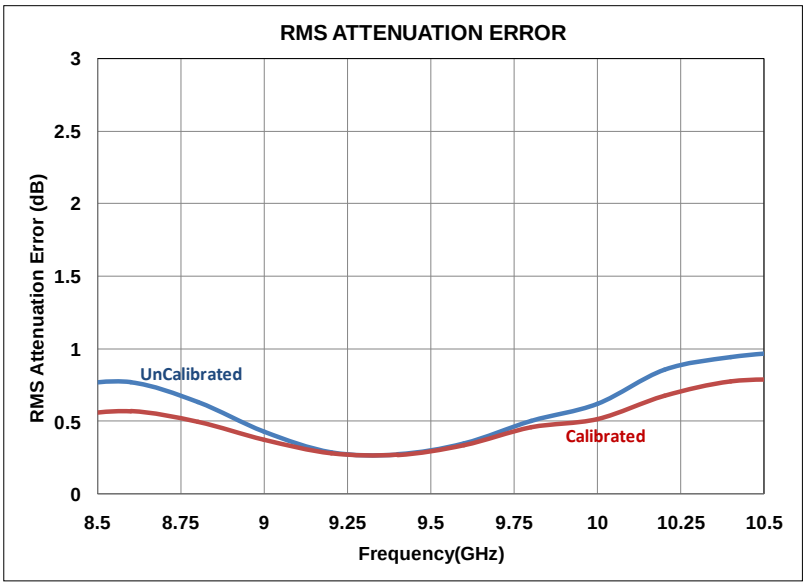
Bit / State (Degree)	Frequency (GHz)		
	9	**9.5**	**10**
5.625	5.8	6.0	6.4
11.25	11.6	11.8	12.3
22.5	21	21.1	20.7
45	46.3	45	45.5
90	90.6	88.5	88.9
180	176.3	178.5	179.3

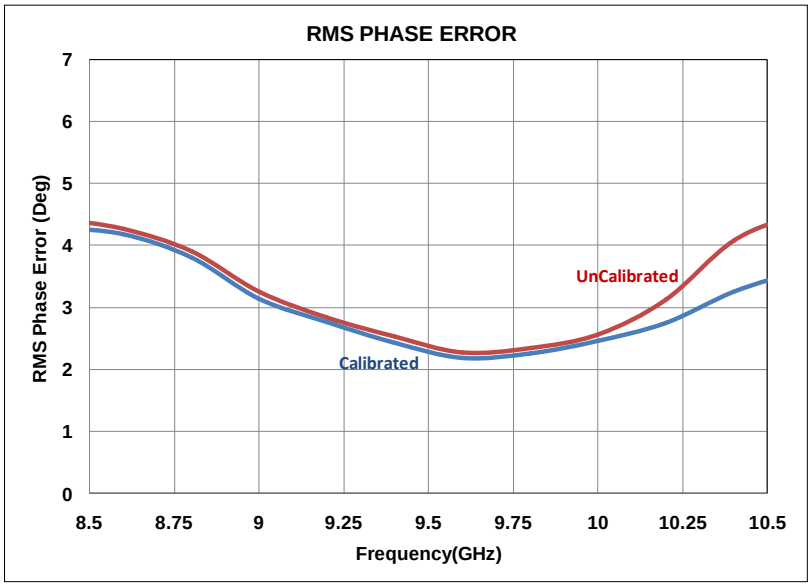
6 Bit Digital Attenuator Performance (only prime states):

Bit / State (dB)	Frequency (GHz)		
	9	**9.5**	**10**
0.5	0.43	0.42	0.44
1	0.92	0.93	0.95
2	2.1	2.05	2.14
4	4.02	3.95	4.12
8	7.8	8.15	8.2
16	15.7	16.35	16.3

Test fixture data in Rx mode (Tx/Rx Control = 0V); Duty cycle = 90%:

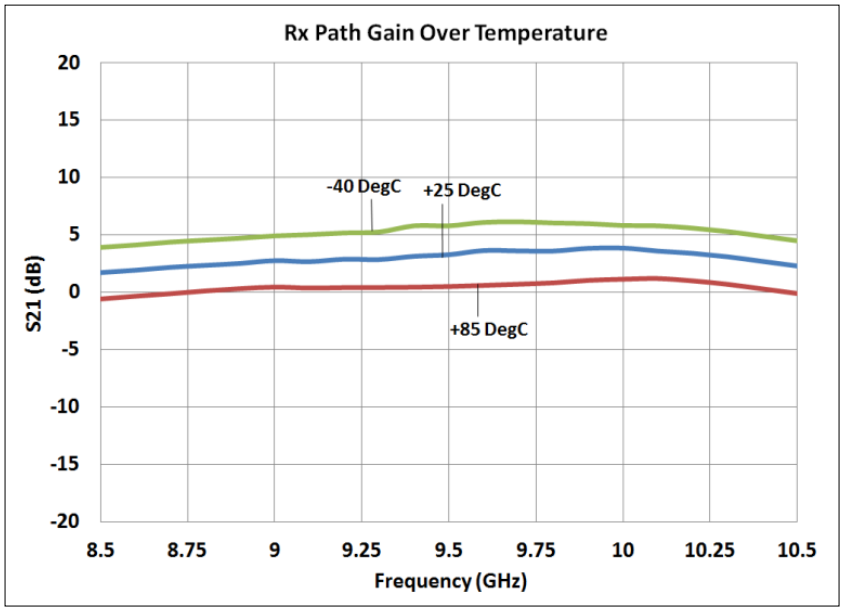
VDDA1 = VDDA2 = 5V ; Total Current ($I_{DDA1Avg}$ + $I_{DDA2Avg}$) = 80mA, T_A = 25 °C

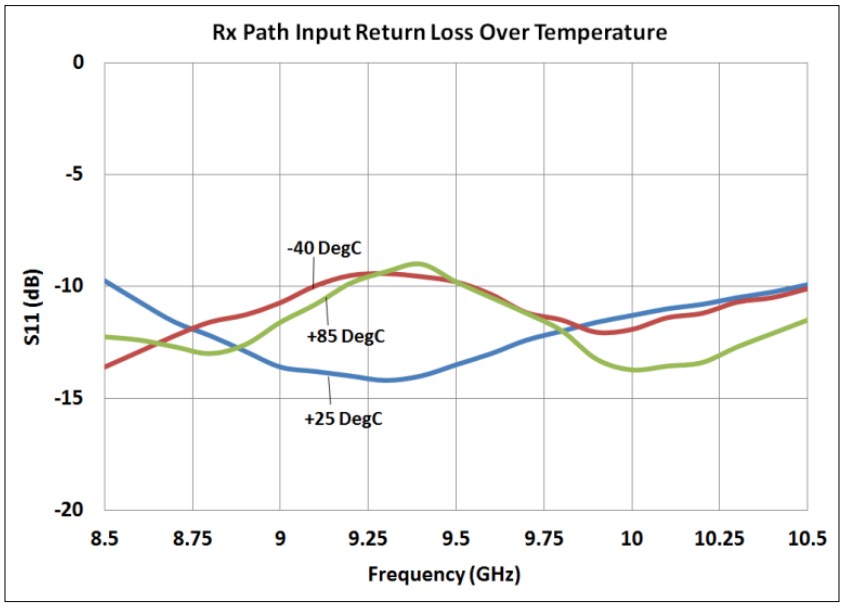




Temperature data in Rx mode (Tx/Rx Control = 0V); Duty cycle = 90%:

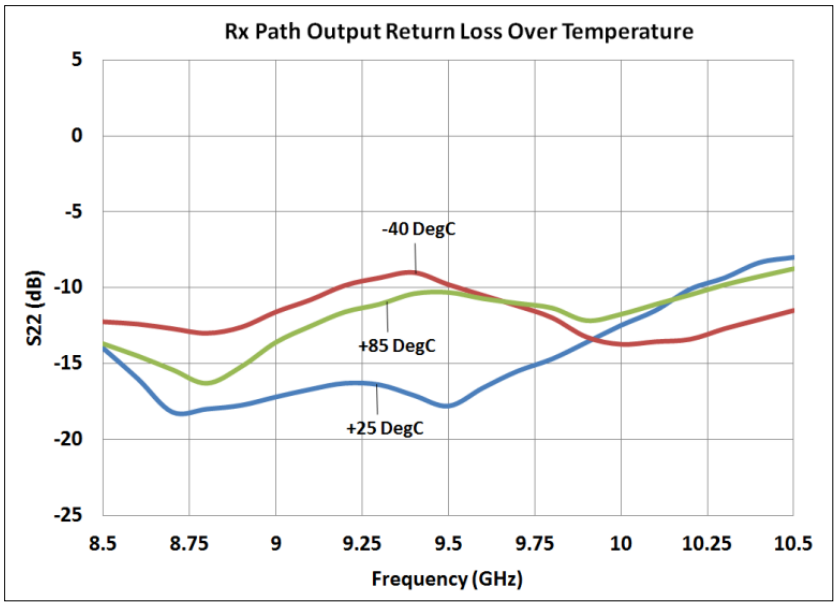
VDDA1 = VDDA2 = 5V ; Total Current ($I_{DDA1Avg}$ + $I_{DDA2Avg}$) = 80mA, T_A = 25 °C





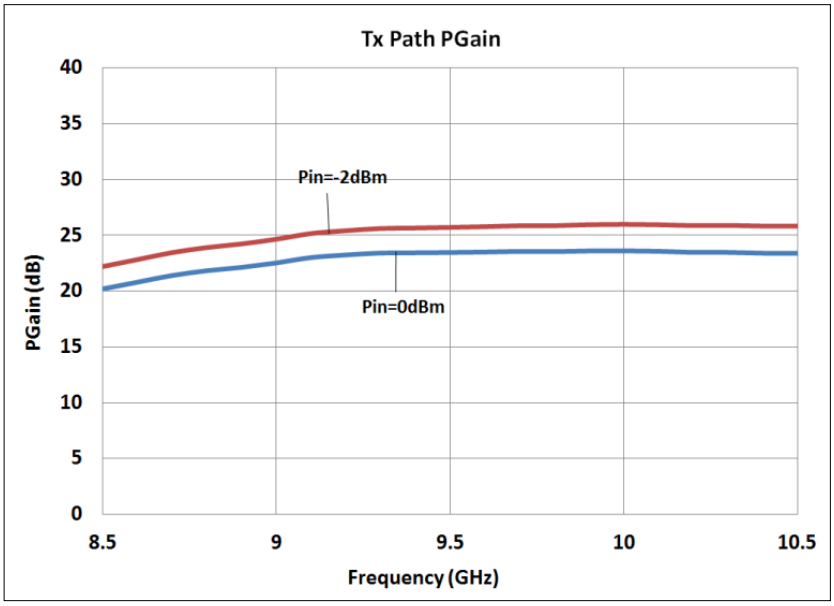
Temperature data in Rx mode (Tx/Rx Control = 0V); Duty cycle = 90%:

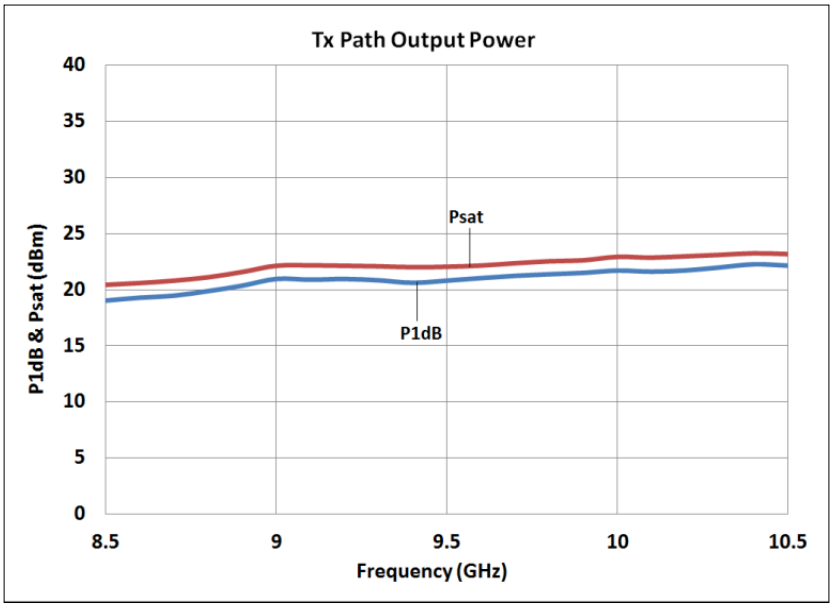
VDDA1 = VDDA2 = 5V ; Total Current ($I_{DDA1Avg}$ + $I_{DDA2Avg}$) = 80mA, T_A = 25 °C



Test fixture data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

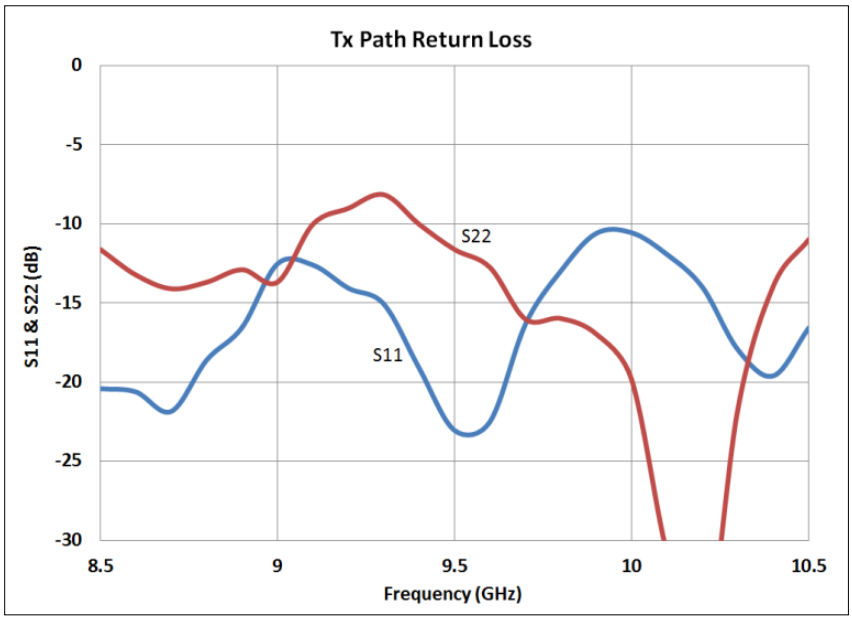
VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -0.9V ; Total Current (I_{Avg}) = 110mA, T_A = 25 °C

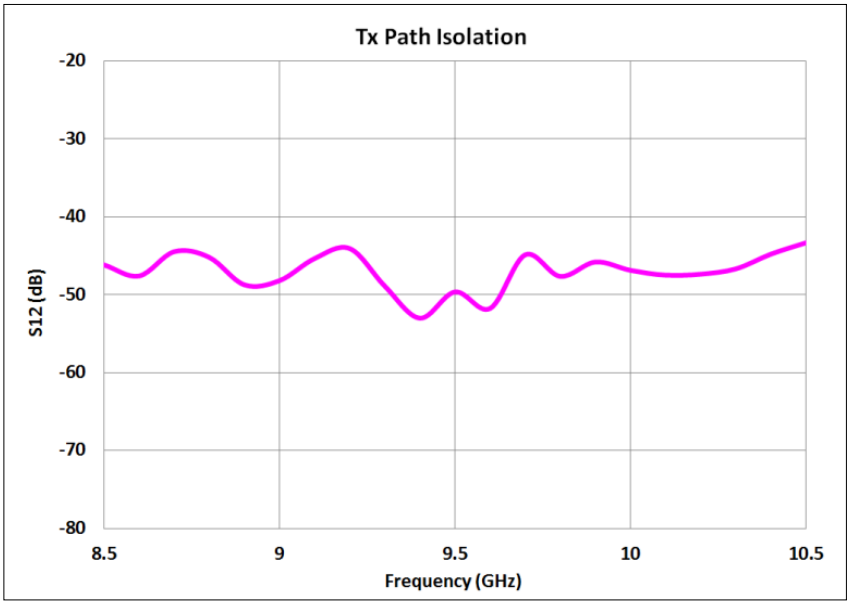




Test fixture data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

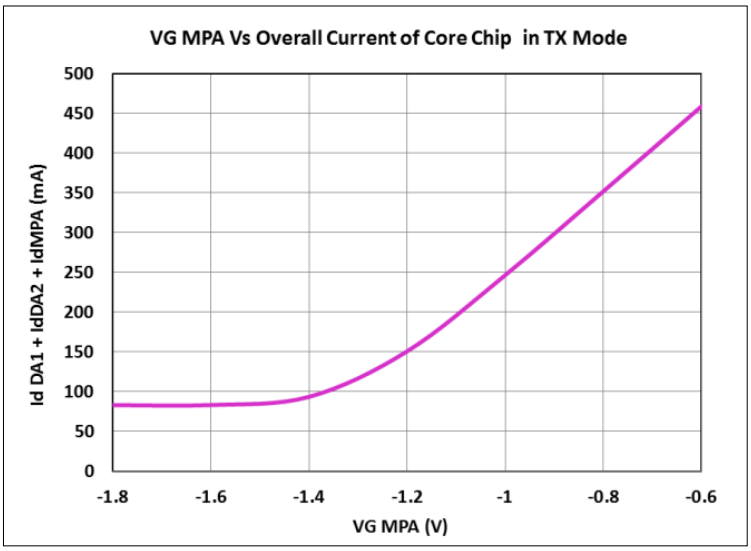
VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -0.9V ; Total Current (I_{Avg}) = 110mA, T_A = 25 °C





Test Fixture data in Tx mode (Tx/Rx Control = 3.3V); CW mode:

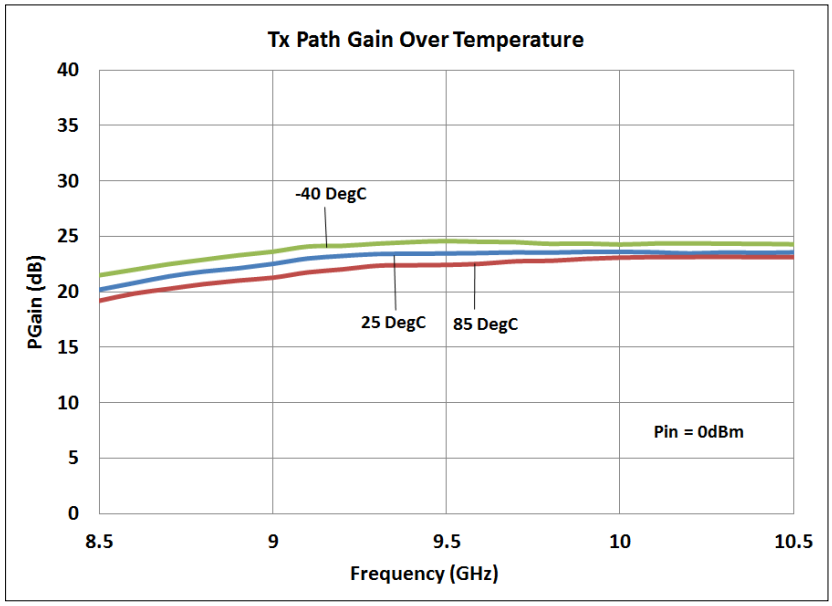
VDDA1 = VDDA2 = VDMPA = 5V ; T_A = 25 °C

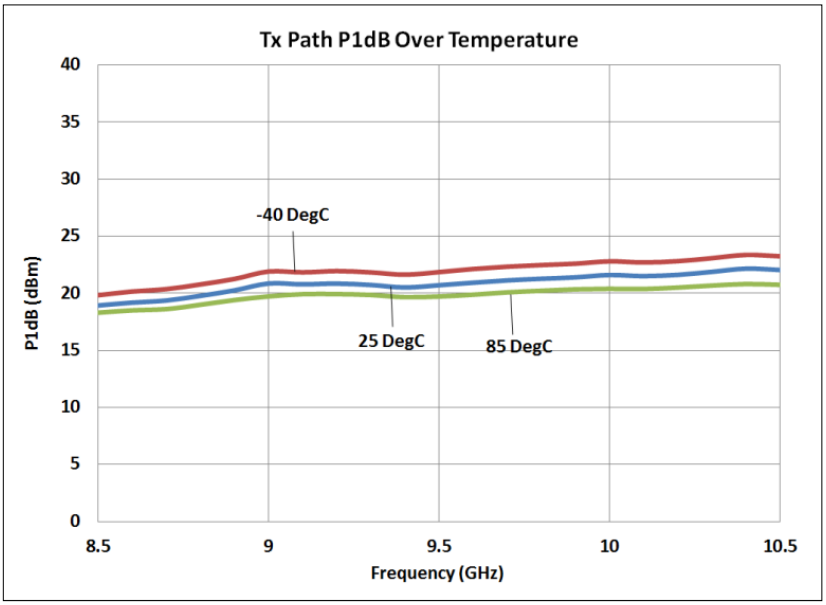


Overall Quiescent Current Variation of Core Chip in Tx Mode by Varying Gate Voltage of MPA (VgMPA).

Temperature data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

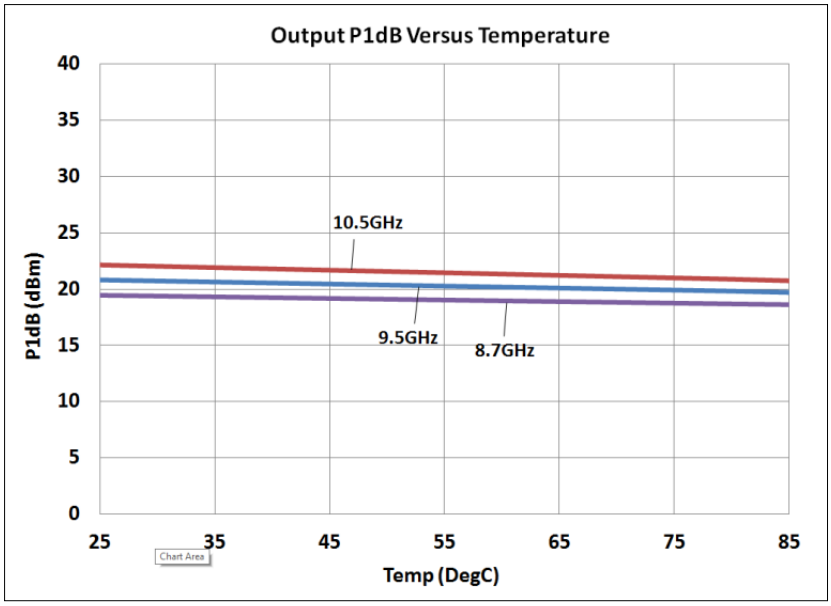
VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -0.9V ; Total Current (I_{Avg}) = 110mA, T_A = 25 °C



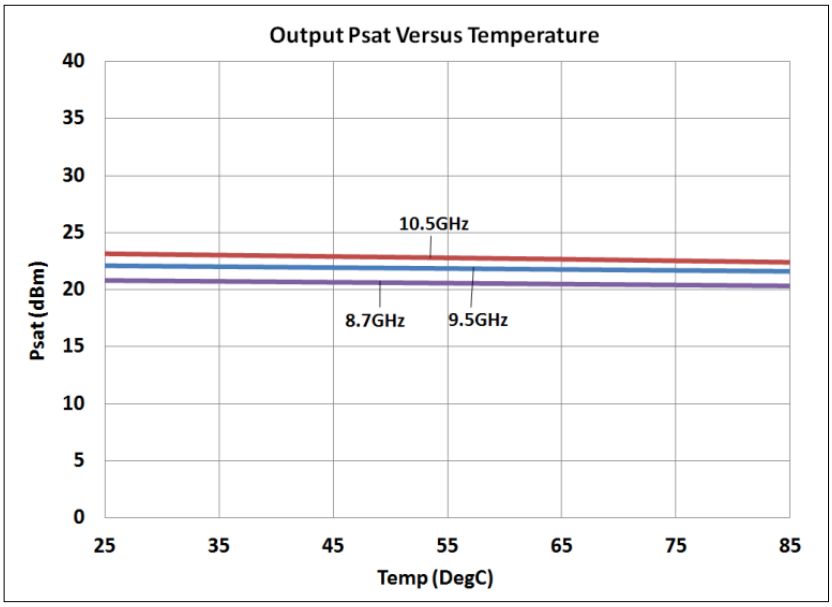


Temperature data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -0.9V ; Total Current (I_{Avg}) = 110mA, T_A = 25 °C



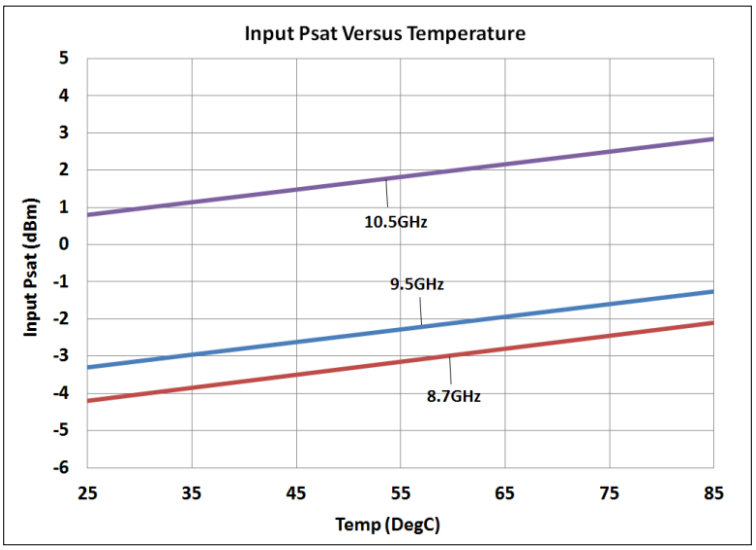
Tx Path Output P1dB Plotted with Temperature on X-Axis



Tx Path Output Psat Plotted with Temperature on X-Axis

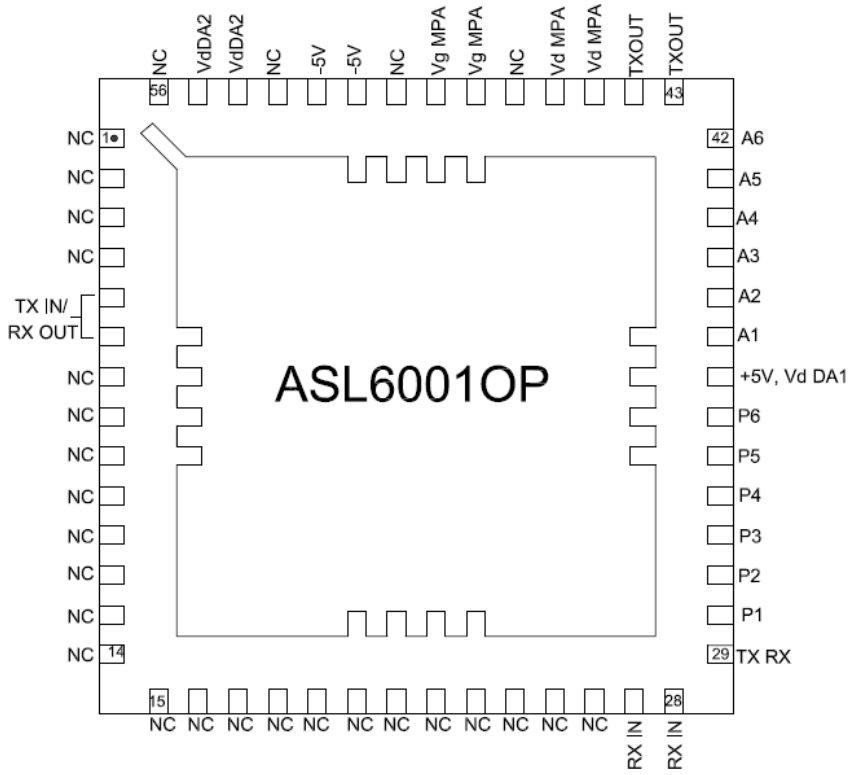
Temperature data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -0.9V ; Total Current (I_{Avg}) = 110mA, T_A = 25 °C



Tx Path Input Psat of Core Chip Plotted with Temperature on X-Axis

Pin details:

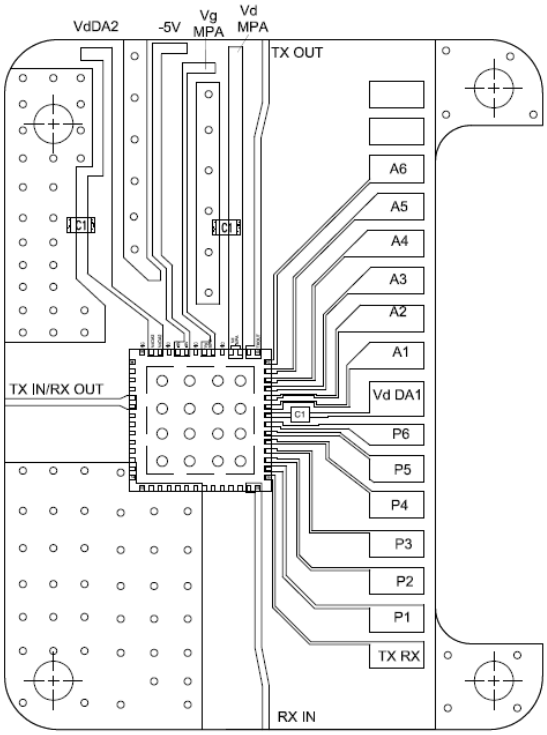


Note:

1. **Pin no. 5, 6 : T_XIN / R_XOUT**
2. **Pin no. 54, 55 : Vd DA2 (Drain Voltage of DA2) = +5V**
3. **Pin no. 51, 52 : -5V (Supply Voltage for Control Ckts and Driver Amplifiers)**
4. **Pin no. 48, 49 : VgMPA (Gate Voltage of MPA) = -0.9V (Typ)**
5. **Pin no. 45, 46 : VdMPA (Drain Voltage of MPA) = +5V**
6. **Pin no. 43, 44 : $T_X$out (Output of the Transmit Path)**
7. **Pin no. 37- 42 : A1-A6 (Attenuator controls) = (3.3- 5V)**
8. **Pin no. 36 : VdDA1 (Drain Voltage of DA1) = +5V**
9. **Pin no. 30- 35 : P6-P1 (Phase shifter controls) = (3.3 – 5V)**
10. **Pin no. 29 : T_X/R_X (T_X/R_X Switch) = (3.3 – 5V)**
11. **Pin no. 27, 28 : R_X IN (Input of the Receive Path)**

All other Pins are NC (No Connection).

Recommended Assembly Diagram:



Note:

1. Input and output 50 ohm lines are preferably on 5 mil RT Duroid substrate.
2. "C1" refers to 0.1uF multilayer chip bypass capacitors for drain supplies corresponding to VdDA1, VdDA2 and VdMPA.
3. TxIN/RxOUT and RxIN ports are DC coupled ports.

Off Chip Components used while recording Test Fixture Data:

Component	Part Number / Description	Vendor
0.1uF MLC Capacitor (C1)	04023C104KAT2A±10%;25V or Equivalent	AVX Corporation

Truth Table for 6 Bit Digital Attenuator:

State	Attenuation (dB)	TTL Control (1 = 3.3 to 5 V, 0 = 0 to 0.2 V)					
		A6 (16)	A5 (8)	A4(4)	A3 (2)	A2(1)	A1 (0.5)
0	0	0	0	0	0	0	0
1	0.5	0	0	0	0	0	1
2	1	0	0	0	0	1	0
4	2	0	0	0	1	0	0
8	4	0	0	1	0	0	0
16	8	0	1	0	0	0	0
32	16	1	0	0	0	0	0
63	31.5	1	1	1	1	1	1

Truth Table for 6 Bit Digital Phase Shifter:

State	Phase (Deg)	TTL Control (1 = 3.3 to 5 V, 0 = 0 to 0.2 V)					
		P6 (180)	P5 (90)	P4(45)	P3 (22.5)	P2(11.25)	P1 (5.625)
0	0	0	0	0	0	0	0
1	5.625	0	0	0	0	0	1
2	11.25	0	0	0	0	1	0
4	22.5	0	0	0	1	0	0
8	45	0	0	1	0	0	0
16	90	0	1	0	0	0	0
32	180	1	0	0	0	0	0
63	354.375	1	1	1	1	1	1

Truth Table for Tx/Rx Switch:

State	Tx Mode / Rx Mode	TTL Control (1 = 3.3 to 5 V, 0 = 0 to 0.2 V)
		TR
0	Rx Mode	0
1	Tx Mode	1

Formulae for RMS Phase or Attenuation Error Calculation:

Formulae for Uncalibrated RMS Error:

$RMS\ Error_{Uncalibrated} = \{(PE_1^2 + PE_2^2 + PE_3^2 \ldots\ldots + PE_{(N-1)}^2)/N\}^{1/2}$

where "PE" is the Phase or Attenuation Error of each individual state.

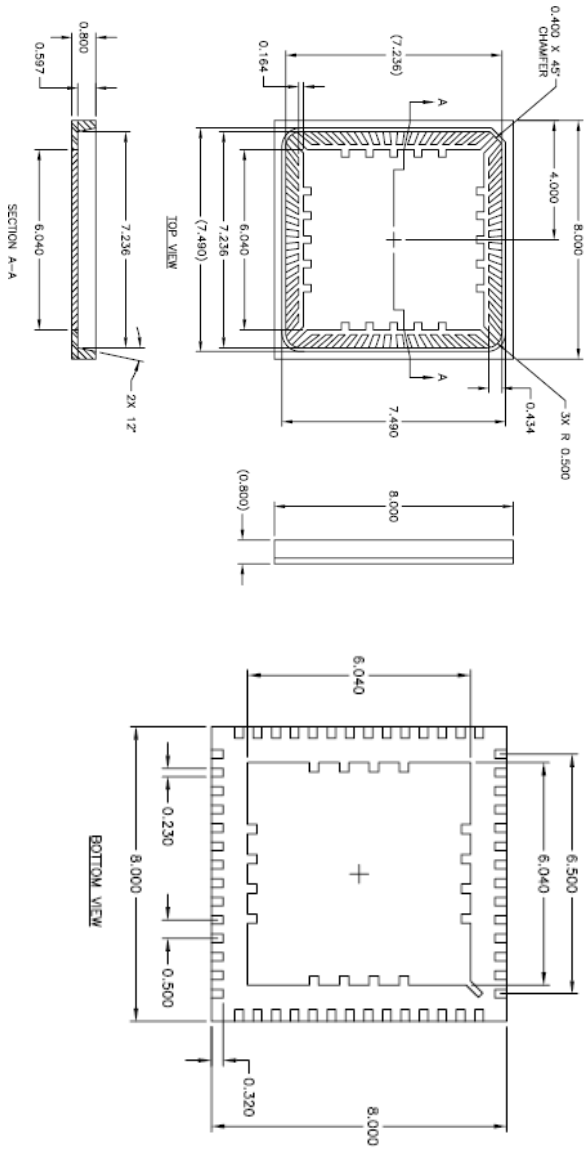
"N" = Total No of States.

Formulae for Calibrated RMS Error:

$RMS\ Error_{calibrated} = [\{(PE_1)^2 + (PE_2)^2 + (PE_3)^2 \ldots\ldots + PE_{(N-1)}^2)/N\} - \{(\sum PE/N)^2\}]^{1/2}$

where "$\sum PE/N$" is the average of sum of each individual Phase or Attenuation Error.

Package outline drawing:



Note: All units are in mm (millimetres).

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice. Please download and refer to datasheet from website before using the product.